AMENDMENTS TO THE CLAIMS

1. (currently amended) A ~~programmable conductor~~ memory cell ~~for an integrated circuit~~, comprising:

a first insulating layer having a top surface and a cell body via;

a memory cell body comprising a glass electrolyte with ~~metal~~ conductive ions disposed therein, the memory cell body being formed entirely within the cell body via and defining a sidewall where the memory cell body and the first insulating layer make contact, the glass electrolyte being capable of selectively precipitating and solubilizing the conductive ions based on an electrical state of the glass electrolyte;

a ~~cathode~~ first electrode in contact with the memory cell body;

a second insulating layer over the first insulating layer extending partially over the top surface of the memory cell body and defining ~~an anode~~ an electrode via to the memory cell body; and

a second electrode ~~an anode~~ in contact with a top surface of the memory cell body and formed in the ~~anode~~ electrode via;

wherein the second electrode ~~anode~~ contacts the top surface of the memory cell body without making contact with ~~contacting~~ the sidewall of the memory cell body.

Claims 2 and 3. (canceled)

4. (currently amended) The ~~programmable conductor~~ memory cell of Claim 52 wherein the spacer comprises an insulating material.

5. (currently amended) The ~~programmable conductor~~ memory cell of Claim 52 wherein the spacer has a thickness extending into the ~~anode~~ electrode via between about 5 nm and 30 nm.

6. (currently amended) The ~~programmable conductor~~ memory cell of Claim 52 wherein the spacer comprises silicon nitride.

7. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1 wherein the memory cell body comprises a plurality of layers.

8. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1 wherein the ~~anode~~ electrode via is filled with metal to form the second electrode.

9. (currently amended) The ~~programmable conductor~~ memory cell of Claim 8 wherein the metal in the ~~anode~~ electrode via is contiguous with a metal layer over the second insulating layer.

10. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1 wherein the ~~cathode~~ first electrode comprises tungsten.

11. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1 wherein the memory cell body comprises a ~~chalcogenide metal ion~~ chalcogenide glass electrolyte material containing conductive ions.

12. (currently amended) The ~~programmable conductor~~ memory cell of Claim 11 wherein the ~~metal~~ conductive ions are chosen from the group of metals consisting of silver, copper, zinc and combinations thereof.

13. (currently amended) The ~~programmable conductor~~ memory cell of Claim 11 wherein the ~~anode~~ second electrode comprises silver.

14. (currently amended) The ~~programmable conductor~~ memory cell of Claim 13 wherein the glass electrolyte material comprises silver-germanium-selenium.

15. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1 wherein a distance between a bottom surface and the top surface of the memory cell body is about 25 nm to 100 nm.

16. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1 wherein a width of the memory cell body via is between about 100 nm and 500 nm.

17. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1, wherein a width of the memory cell body via is between about 200 nm and 300 nm.

18. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1, wherein the first insulating layer comprises silicon nitride.

19. (currently amended) The ~~programmable conductor~~ memory cell of Claim 18, wherein the first insulating layer has a thickness between about 10 nm and 200 nm.

20. (currently amended) The ~~programmable conductor~~ memory cell of Claim 18, wherein the first insulating layer has a thickness between about 25 nm and 150 nm.

21. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1, wherein the second insulating layer comprises silicon nitride.

22. (currently amended) The ~~programmable conductor~~ memory cell of Claim 21 wherein the second insulating layer has a thickness between about 50 nm and 200 nm.

23. (currently amended) The ~~programmable conductor~~ memory cell of Claim 21, wherein the second insulating layer has a thickness between about 80 nm and 150 nm.

24. (currently amended) The ~~programmable conductor~~ memory cell of Claim 52 wherein the ~~anode~~ electrode via has a width no greater than a width of the cell body via.

Claims 25-48. (canceled)

49. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1, wherein the memory cell body fills the cell body via.

50. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1, wherein the top surface of the memory cell body is coplanar with the top surface of the first insulating layer.

51. (currently amended) The ~~programmable conductor~~ memory cell of Claim 1, wherein the ~~cathode~~ first electrode extends outside the sidewall of the memory cell body.

52. (currently amended) A ~~programmable conductor~~ memory cell ~~for an integrated circuit~~, comprising:

a first insulating layer having a top surface and a cell body via;

a memory cell body comprising a glass electrolyte with ~~metal~~ conductive ions disposed therein , the glass electrolyte being capable of selectively precipitating and solubilizing the conductive ions based on an electrical state of the glass electrolyte, the memory cell body being contained within the cell body via and defining a sidewall where the memory cell body and the first insulating layer make contact;

a ~~cathode~~ first electrode in contact with the memory cell body;

a second insulating layer over the first insulating layer and defining an ~~anode~~ electrode via to the memory cell body;

a second electrode ~~an anode~~ in contact with a top surface of the memory cell body and formed in the ~~anode~~ electrode via;

wherein the ~~anode~~ electrode via has a width about the same as a width of the memory cell body, and the ~~anode~~ electrode via is lined with a spacer that covers a sidewall edge of the memory cell body, such that the a second electrode ~~anode~~ contacts the top surface of the memory cell body without contacting the sidewall of the memory cell body.

53. (currently amended) The ~~programmable conductor~~ memory cell of Claim 52, wherein the ~~anode~~ electrode via is filled with metal to form the second electrode.

54. (currently amended) The ~~programmable conductor~~ memory cell of Claim 52, wherein the ~~cathode~~ first electrode comprises tungsten.

55. (new) The memory cell of Claim 1, wherein the first electrode is a cathode.

56. (new) The memory cell of Claim 1, wherein the second electrode is an anode.

57. (new) The memory cell of Claim 52, wherein the first electrode is a cathode.

58. (new) The memory cell of Claim 52, wherein the second electrode is an anode.